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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G06F 15/00, 15/76, 15/80, H04Q 11/04, G06F 7/00 — A1

(11) International Publication Number: WO 97/04397

(43) International Publication Date: 6 February 1997 (06.02.97)

(21) International Application Number: PCT/US96/11946

(22) International Filing Date: 18 July 1996 (18.07.96)

(30) Priority Data:
60/001,498 19 July 1995 (19.07.95) US

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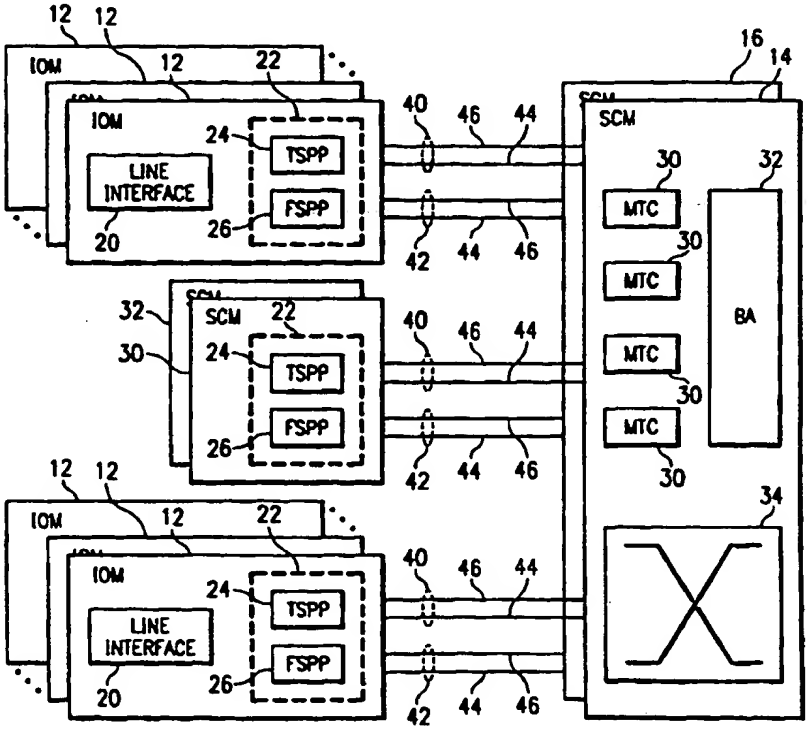
(81) Designated States: AL, AM, AT, AU, AZ, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: SERIAL CONTROL AND DATA INTERCONNECT SYSTEM USING A CROSSBAR SWITCH AND A MULTIPOINT TOPOLOGY

(57) Abstract

A communication device (10) includes a number of input/output modules (12) coupled to a switch control module (14) using an interconnect (40) and to a redundant switch control module (16) using a redundant interconnect (42). Each interconnect (40) and redundant interconnect (42) includes a control interconnect (44) and a data interconnect (46). The control interconnect (44) establishes control information for transferring a cell in the communication device (10) and the data interconnect (46) performs the cell transfer.



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SERIAL CONTROL AND DATA INTERCONNECT SYSTEM USING A CROSSBAR SWITCH AND A MULTIPOINT TOPOLOGY

RELATED APPLICATIONS

This application claims the benefit of United States Provisional Application Serial No. 60/001,498, filed July 19, 1995.

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to communication systems, and more specifically to a serial control and data interconnect.

BACKGROUND OF THE INVENTION

A communication system includes a collection of components that communicate, manipulate, and process information in a variety of ways. The system may support different access technologies, such as frame relay, circuit services, and new and evolving connection-based or connectionless services, that communicate information, such as data, voice, and video. Switches in the communication system employ hardware and software to route information generated by access technologies to an intended destination. In an integrated services network, switches may route information among access technologies in a unified manner.

With an increasing demand for more sophisticated and higher bandwidth communication, switches in a communication system must be scalable and adaptable to the particular needs of the users. Also, switches should support existing access technologies, and provide a flexible framework for new and evolving services.

Existing switches in an integrated services environment suffer from several disadvantages. Switches fail to be modular and scalable to adapt, for example, to the needs and resources of a small private network serving hundreds of users, as well as a larger public network serving tens of thousands of users. Often, switches only support one or a few number of access technologies and offer limited expansion capabilities. Also, as integrated services networks get larger and more complex, existing switches may fail to provide adequate redundancy and fault isolation.

SUMMARY OF THE INVENTION

In accordance with the present invention, the disadvantages and problems associated with switches in a communication system has been substantially reduced or eliminated. In particular, a communication device routes information generated by a variety of access technologies, and includes serial control and data interconnects among its modules to provide modularity, scalability, redundancy, and improved fault isolation.

In accordance with one embodiment of the present invention, a communication device includes a switch control module having a switch fabric and a number of input/output modules having cell flow processors. Control interconnects couple cell flow processors of the input/output modules to the switch fabric of the switch control module. Data interconnects couple cell flow processors of the input/output modules to the switch fabric of the switch control module.

Important technical advantages of the present invention include an architecture of a communication device that provides modularity, scalability, redundancy, and improved fault isolation. In particular, a communication device includes a switch control module coupled to a number of input/output modules using control and data interconnects that operate in a serial fashion to reduce connection complexity and size. In a specific implementation, each input/output module is coupled to a switch control module using a dedicated seven-line serial control interconnect and a dedicated four-line serial data interconnect. This connectivity scheme avoids the complexity, inefficiency, and increased cost of a common or

shared bus architecture, while supporting additional input/output modules. A redundant switch control module can also couple to the input/output modules for increased reliability. The serial control and data interconnects improve fault isolation through parity checking. Other technical advantages are readily apparent to one skilled in the art from the following figures, descriptions, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and for further features and advantages, reference is now made to the following written description taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates a communication device;

FIGURE 2 illustrates the connectivity scheme among components of the communication device;

FIGURE 3 illustrates in more detail a control interconnect between components in the communication device;

FIGURE 4 illustrates in more detail a data interconnect between components in the communication device; and

FIGURE 5 illustrates a timing diagram for communications using the data interconnect.

DETAILED DESCRIPTION OF THE INVENTION

FIGURE 1 illustrates a communication device 10 that includes a plurality of input/output modules (IOMs) 12 coupled to a switch control module (SCM) 14. In a particular embodiment, a redundant SCM 16 is also coupled to IOMs 12. In operation, IOMs 12 receive information, such as voice, video, and data, using a variety of access technologies. This information is passed to SCM 14 and routed through a selected IOM 12 to an intended destination.

Each IOM 12 includes zero or more line interfaces 20 and a cell flow processor 22 having a to-switch port processor (TSPP) 24 and a from-switch port processor (FSPP) 26. In one embodiment, line interface 20 includes a connectivity engine, network interworking, and physical interface to receive data from and provide data to a variety of access technologies. For example, line interface 20 may support asynchronous transfer mode (ATM) cell relay (OC-12, OC-3c, 155 Mbps UTP), frame relay (T1, E1, T3, E3, V.35), circuit emulation (T1, E1, T3, E3), internetworking using Ethernet, Fast Ethernet, Internet Protocol (IP), or IP over ATM, or any other communications protocol or access technology. Communication device 10 contemplates line interface 20 that supports any suitable communication technique, whether connection-based or connectionless.

The structure and function of line interface 20 may vary between IOMs 12 to provide modular support for different access technologies. For example, communication device 10 may include an IOM 12 to support ATM, another IOM 12 to support frame relay, still another IOM 12 to support

an internetworking function with an Ethernet local area network (LAN), and any other suitable IOM 12. Communication device 10 contemplates any number and arrangement of IOMs 12 to support different access technologies. Line interface 20 may include one or more components in hardware or software and, in a particular example, includes one or more application specific integrated circuits (ASICs).

Cell flow processor 22 provides an interface between line interface 20 and SCM 14. Unlike line interface 20 which may vary for different access technologies, cell flow processor 22 has the same structure and performs the same function for all IOMs 12. In a particular embodiment, cell flow processor 22 implements a core cell transfer function using ATM with virtual channel (VC) accounting and buffer control. Each cell flow processor 22 includes TSPP 24 for communications into SCM 14 and FSPP 26 for communications from SCM 14. In a particular implementation, TSPP 24 and FSPP 26 comprise an ASIC. Both SCM 14 and redundant SCM 16 may have portions 30 and 32, respectively, that include cell flow processor 22. This allows SCM 14 and redundant SCM 16 to communicate information among components in communication device 10 in the same manner as IOMs 12. Each cell flow processor 22 corresponds to a port or switch port in communication device 10.

Cell flow processors 22 residing on IOMs 12 provide a distributed cell processing architecture that reduces the complexity of SCM 14 and enhances the modularity and scalability of communication device 10. In particular, each IOM 12 added to communication device 10 as an upgrade or to enhance capacity includes its own cell flow processor

22. The on-board cell flow processor 22 of IOMs 12 reduces complexity and cost of entry-level systems, and also establishes a common and consistent interface between IOMs 12 and SCM 14. Therefore, IOMs 12 may be developed for new or evolving access technologies by combining a different structure and function for line interface 20 with the established structure and function for cell flow processor 22 for easy integration into communication device 10.

SCM 14 includes a number of multi-point topology controllers (MTCs) 30, a bandwidth arbiter (BA) 32, and a data crossbar 34, all making up a switch fabric 35. MTC 30 may comprise an ASIC that communicates with a selected number of IOMs 12 and centralizes state information needed for multi-point topology supported by communication device 10. Since IOMs 12 provide access to both connection-based and connectionless environments, MTCs support point-to-point (P2P), multipoint-to-point (M2P), point-to-multipoint (P2M), and multipoint-to-multipoint (M2M) communications. BA 32 accumulates and arbitrates transfer requests from each IOM 12. Specifically, BA 32 directs input/output mapping of data crossbar 34 on a per cell-time basis, dynamically schedules momentarily unused bandwidth of communication device 10, and resolves M2P bandwidth contention. Redundant SCM 16 includes the same components and operates in the same fashion as SCM 14.

One particular technical advantage of communication device 10 is the interconnection between IOMs 12, SCM 14, and redundant SCM 16. Each IOM 12 couples to SCM 14 using interconnect 40 and to redundant SCM 16 using redundant interconnect 42. Both interconnect 40 and redundant interconnect 42 include control interconnect 44 and data

interconnect 46, which are dedicated connections since they support communication between SCM 14 and the associated IOM 12. Each portion 30 and 32 of SCM 14 and redundant SCM 16, respectively, may also include interconnect 40 and redundant interconnect 42.

Control interconnect 44 and data interconnect 46 operate serially and, therefore, reduce the connection complexity and size between IOMs 12 and SCM 14 in communication device 10. As described below, the serial operation of control interconnect 44 and data interconnect 46 enhances the modularity and scalability of communication device 10. Control interconnect 44 and data interconnect 46 reduce or eliminate the need for an expensive and complicated common or shared bus architecture in communication device 10. Also, the reduced number of lines in control interconnect 44 and data interconnect 46 simplifies fault isolation. For example, information communicated on these serial lines may include one or more parity bits to quickly and efficiently identify faulty components in communication device 10.

FIGURE 2 illustrates a connectivity scheme used by communication device 10. This connectivity scheme represents the interconnections established by a backplane 48 or other similar device in the chassis or support structure of communication device 10. IOMs 12, SCM 14, and redundant SCM 16 may be integrated circuit boards that plug into slots in backplane 48 to effect the connectivity scheme. Backplane 48 or other similar device implements the specified connections between components in communication device 10 to establish interconnects 40 and redundant interconnects 42.

Each IOM 12 includes a connector region 50 and a redundant connector region 52. SCM 14 and redundant SCM 16 include connector regions 54 and redundant connector regions 56. Connector regions 50, 52, 54, and 56 represent a collection of contiguous or non-contiguous pins, conductors, or other matings on components in communication device 10.

Connector region 50 of each IOM 12 is coupled to and has a one-to-one correspondence with an associated connector region 54 on SCM 14 to establish interconnect 40. Likewise, redundant connection region 52 of each IOM 12 is coupled to and has a one-to-one correspondence with an associated connection region 54 of redundant SCM 16 to establish redundant interconnect 42. Therefore, each interconnect 40 establishes a dedicated communication path or link between an associated IOM 12 and SCM 14, and each redundant interconnect 42 establishes a dedicated communication path or link between an associated IOM 12 and redundant SCM 16. Throughout this description, interconnect 40, redundant interconnect 42, control interconnect 44, and data interconnect 46 may represent connection regions, lines, pins, conductors, matings, connectors, or any combination of these elements to accomplish a coupling between components in communication device 10.

Since SCM 14 and redundant SCM 16 may include a cell flow processor 22, the connectivity scheme includes two additional redundant interconnects 42a and 42b. In particular, cell flow processor 22 on portion 32 of redundant SCM 16 is coupled to a corresponding connection region 54 on SCM 14 using redundant connection region 56 on

redundant SCM 16 to establish redundant interconnect 42a. Likewise, cell flow processor 22 on portion 30 of SCM 14 is coupled to a corresponding connection region 54 on redundant SCM 16 using redundant connection region 56 on SCM 14 to establish redundant interconnect 42b.

The connectivity scheme illustrated in FIGURE 2 provides several advantages to communication device 10. SCM 14 and redundant SCM 16 may include many connection regions 54 that support a number of existing or potential IOMs 12. However, each IOM 12 maintains one connection region 50 and one redundant connection region 52 to establish interconnect 40 and redundant interconnect 42, respectively, which reduces the cost and complexity of backplane 48. This dedicated connection approach instead of a common or shared bus approach improves modularity and scalability. In particular, an entry-level communication device 10 may include SCM 14 and eight IOMs 12, but with a backplane 48 of reduced complexity and size that still accommodates future upgrades and additions. Depending upon its requirements and demands, a user of communication device 10 may add redundant SCM 16 to enhance reliability or add more IOMs 12 to improve capacity or support a different access technology.

FIGURE 3 illustrates in more detail control interconnect 44 between IOMs 12 and SCM 14. A similar control interconnect 44 exists between IOMs 12 and redundant SCM 16. Each control interconnect 44 includes two lines, conductors, couplings, connectors, matings, or connections (referred to generally as lines) between TSPP 24 of IOM 12 and an associated MTC 30 of SCM 14: a line from TSPP 24 to MTC 30 (T2M) 60 and a line from MTC 30 to

TSPP 24 (M2T) 62. Control interconnect 44 also includes two lines between FSPP 26 and MTC 30: a line from FSPP 26 to MTC 30 (F2T) 64 and a line from MTC 30 to FSPP 26 (M2F) 66. Also, control interconnect 44 includes a line from TSPP 24 to BA 32 (T2B) 68. In a particular implementation, T2M 60 and M2T 62 comprise two lines each, whereas F2M 64, M2F 66, and T2B 68 comprise one line each. Therefore, in this particular embodiment, control interconnect 44 comprises seven lines between IOM 12 and SCM 14. Another seven lines from IOM 12 may establish a similar control interconnect 44 with redundant SCM 16.

Each MTC 30 may support several IOMs 12. In a particular implementation, each MTC 30 supports four IOMs, resulting in twenty-four lines to implement four control interconnects 44. MTC 30 communicates with BA 32 using control line 70. Control line 70 comprises sixteen lines from MTC 30 to BA 32 and nine lines from BA 32 to MTC 30. In a system that includes sixteen IOMs 12 and four MTCs 20, BA 32 receives and transmits control information relating to the operation of communication device 10 on eighty input lines (twenty-four lines for each control line 70 and one line for each T2B 68) and four output lines (one line for each control line 70).

In operation, communication device 10 using control interconnect 44 manages communications between receive IOM 12a and transmit IOM 12b. For a P2P cell transfer, line interface 20 receives information in the format or protocol used by the access technology supported by IOM 12a. Line interface 20 translates this information into the core cell transfer format supported by cell flow processor 22. TSPP 24 receives the cell and generates a request for

communication over T2B 68 for a designated output port. BA 32 grants the request and communicates the grant to TSPP 24 using control line 70, MTC 30, and M2T 62.

MTC 30 then performs any necessary translation to identify the virtual channel (VC) queue associated with transmit IOM 12b. Each TSPP 24 transmits a scheduling list number to the MTC 30 on the T2M line 60. The scheduling list number reflects the connection it is transferring a cell from. The MTC 30 uses this information to determine the output port(s) and multiQueue number(s) to which the cell will be transferred. The MTC 30 passes this information to the BA 32 on the M2B lines 70, and the BA 32 passes the multiQueue number to the MTC(s) on the B2M lines 70. The MTC 30 further passes the multiQueue number(s) to the FSPP(s) 26 using the M2F line 66. The FSPP 26 uses multiQueue number to determine which output queue(s) are to receive the cell and whether these queues are full. Flow control information, based on the queue status is communicated in the reverse direction, i.e. F2M 64, followed by M2B 70, followed by B2M 70, and lastly M2T 62. This control information happens in parallel for all port processors, and control flow is capable of multipoint transfers.

FIGURE 4 illustrates in more detail data interconnect 46 that transfers the cell after establishing the appropriate control information using control interconnect 44. Shown in more detail in IOM 12 is TSPP 24 coupled to a serializer 80 and FSPP 26 coupled to a deserializer 82. In a particular embodiment, serializer 80 and deserializer 82 support a fiber channel high speed serial interface. Serializer 80 converts an n-bit word received from TSPP 24

into a differential emitter coupled logic (ECL) signal for transmission over transmit line pair 84. Transmit line pair 84 is coupled to input port 86 of data crossbar 34. Output port 88 of data crossbar 34 is coupled to a differential ECL receive line pair 90, which in turn is coupled to deserializer 82 in IOM 12. Deserializer 82 converts information received over receive line pair 90 into an n-bit word for delivery to FSPP 26.

In this embodiment, data crossbar 34 includes input port 86 and an associated output port 88 for each IOM 12 coupled to SCM 14. Input port 86 and output port 88 each comprise a line pair connection. Data crossbar 34 may be an ECL cross-point device under the control of BA 32. Upon receiving the appropriate control information established using control interconnect 44, BA 32 configures data crossbar 34 to achieve the proper cell transfer. Data crossbar 34 maps one input port 86 to one or more output ports 88. For example, data crossbar 34 may establish a connection between input port 86 associated with IOM 12a and output port 88 associated with IOM 12b. In another example, data crossbar 34 may establish a connection between input port 86 and output port 88 associated with the same IOM 12.

In a particular implementation, TSPP 24 and FSPP 26 on IOM 12 operate using a fifty MHZ system clock. Data is transferred in a twenty bit word to serializer 80 and converted into a one GHz differential ECL signal for transfer over transmit line pair 84 to data crossbar 34. Data crossbar 34 simultaneously supports sixteen ports or IOMs 12, and additional data crossbars 34 may be added to increase the capacity of SCM 14. Data crossbar 34 performs

high speed switching between input ports 86 and associated output ports 88 under the direction of BA 32. Receive line pair 90 communicates information from output port 88 to deserializer 82, which converts the one GHz differential ECL signal into a twenty bit digital word at fifty MHZ for presentation to FSPP 26.

To accommodate high bandwidth traffic, transmit line pair 84 and receive line pair 90 of data interconnect 46 are high speed serial links. With increased data rates of one GHz or more, communication device 10 may experience a clock skew problem caused by communication delays in transmit line pair 84 and receive line pair 90. Therefore, communication device 10, and specifically deserializer 82, employs a phase lock loop and resynchronizer to account for clock skew over data interconnect 46.

FIGURE 5 illustrates a timing diagram for transfer of a cell from TSPP 24 TO FSPP 26 using data interconnect 46. A cell clock pulse 102 occurs every thirty-two cycles of system clock 104 which, in a particular implementation, operates at fifty MHZ. Each cell clock pulse 102 represents a single cell transfer and receive event using data interconnect 46.

A signal 106 generated by serializer 80 for transmission over transmit line pair 84 begins with a preamble 108 which, in a particular embodiment, comprises a serial bit stream of alternating "1s" and "0s." A phase lock loop in deserializer 82 establishes synchronization with the one GHz signal using preamble 108. After preamble 108, serializer 80 generates a sync 110 that indicates the beginning of data 112. Serializer 80 concludes the transmission during cell clock pulse 102 with a postamble

114 that, like preamble 108, includes a serial bit stream of alternating "1s" and "0s" to allow synchronization by deserializer 82.

Deserializer 82 receives a signal 116, which includes preamble 108, sync 110, data 112, and postamble 114. A sufficient length of postamble 114 from the previous cell and preamble 108 from the current cell before sync 110 ensures that deserializer 82 is in sync with the one GHz signal and ready to receive data 112. Between cells, BA 32 reconfigures data crossbar 34 to deliver the next cell of information.

Although the present invention has been described in several embodiments, a myriad of changes, variations, alterations, transformations, and modifications may be suggested to one skilled in the art, and it is intended that the present invention encompass such changes, variations, alterations, transformations, and modifications as fall within the spirit and scope of the appended claims.

WHAT IS CLAIMED IS:

1. A communication device comprising:

a switch control module having a switch fabric;

a plurality of input/output modules, each input/output module having a cell flow processor;

a plurality of control interconnects, each control interconnect operable to couple a cell flow processor of an input/output module to the switch fabric of the switch control module; and

a plurality of data interconnects, each data interconnect operable to couple a cell flow processor of an input/output module to the switch fabric of the switch control module.

2. The device of Claim 1, wherein the switch control module further comprises a plurality of multipoint topology controllers coupled to the bandwidth arbiter, each multipoint topology controller operable to couple to at least one cell flow processor of an input/output module.

3. The device of Claim 1, wherein the switch control module further comprises a cell flow processor, wherein the cell flow processor of the switch control module is coupled to the bandwidth arbiter of the switch control module.

4. The device of Claim 1, further comprising:

a redundant switch control module having a switch fabric;

a plurality of redundant control interconnects, each redundant control interconnect operable to couple a cell flow processor of an input/output module to the switch fabric of the redundant switch control module; and

a plurality of redundant data interconnects, each redundant data interconnect operable to couple a cell flow processor of an input/output module to the switch fabric of the redundant switch control module.

5. The device of Claim 1, wherein each cell flow processor further comprises:

a to-switch port processor; and

a from-switch port processor.

6. The device of Claim 5, wherein each data interconnect comprises:

two lines operable to couple the to-switch port processor of the input/output module to the switch fabric of the switch control module; and

two lines operable to couple the from-switch port processor of the input/output module to the switch fabric of the switch control module.

7. The device of Claim 5, wherein each data interconnect comprises:

two differential emitter coupled logic lines operable to couple the to-switch port processor of the input/output module to the switch fabric of the switch control module; and

two differential emitter coupled logic lines operable to couple the from-switch port processor of the input/output module to the switch fabric of the switch control module.

8. The device of Claim 5, wherein the switch control module further comprises a plurality of multipoint topology controllers coupled to the bandwidth arbiter, each multipoint topology controller operable to couple to at least one cell flow processor of an input/output module, each control interconnect comprising:

four lines operable to couple the to-switch port processor of the input/output module to an associated multipoint topology controller of the switch control module;

two lines operable to couple the from-switch port processor of the input/output module to the associated multipoint topology controller of the switch control module; and

one line operable to couple the to-switch port processor of the input/output module to the bandwidth arbiter of the switch control module.

9. A communication device comprising:

a switch control module having a switch fabric and a plurality of first connector regions;

a plurality of input/output modules, each input/output module having a second connector region coupled to a cell flow processor, each second connector region coupled to and having a one-to-one correspondence with a first connector region of the switch control module.

10. The device of Claim 9, further comprising a redundant switch control module having a switch fabric and a plurality of third connector regions, each input/output module having a fourth connector region coupled to the cell flow processor, each fourth connector region coupled to and having a one-to-one correspondence with a third connector region of the redundant switch control module.

11. The device of Claim 10, wherein the switch control module further comprises a fifth connection region coupled to a cell flow processor of the switch control module, the fifth connection region coupled to and having a one-to-one correspondence with a third connector region of the redundant switch control module.

12. The device of Claim 9, further comprising a backplane having a plurality of interconnects, each interconnect operable to couple a first connector region to a corresponding second connector region, each interconnect comprising a data interconnect and a control interconnect.

13. The device of Claim 12, wherein each cell flow processor further comprises a to-switch port processor and a from-switch port processor, each data interconnect comprises:

two lines operable to couple the to-switch port processor of the input/output module to the switch fabric of the switch control module; and

two lines operable to couple the from-switch port processor of the input/output module to the switch fabric of the switch control module.

14. The device of Claim 12, wherein each cell flow processor further comprises a to-switch port processor and a from-switch port processor, each data interconnect comprises:

two differential emitter coupled logic lines operable to couple the to-switch port processor of the input/output module to the switch fabric of the switch control module; and

two differential emitter coupled logic lines operable to couple the from-switch port processor of the input/output module to the switch fabric of the switch control module.

15. The device of Claim 12, wherein each cell flow processor further comprises a to-switch port processor and a from-switch port processor, wherein the switch control module further comprises a plurality of multipoint topology controllers coupled to a bandwidth arbiter, each multipoint topology controller coupled to at least one cell flow processor of an input/output module, each control interconnect comprising:

four lines operable to couple the to-switch port processor of the input/output module to an associated multipoint topology controller of the switch control module;

two lines operable to couple the from-switch port processor of the input/output module to the associated multipoint topology controller of the switch control module; and

one line operable to couple the to-switch port processor of the input/output module to the bandwidth arbiter of the switch control module.

16. An input/output module operable to couple to a switch control module having a switch fabric, the input/output module comprising:

a line interface;

a to-switch port processor;

a from-switch port processor;

a data interconnect coupled to the to-switch processor and the from-switch processor, the data interconnect operable to couple to the switch fabric of the switch control module; and

a control interconnect coupled to the to-switch port processor and the from-switch port processor, the control interconnect operable to couple to the switch fabric of the switch control module.

17. The input/output module of Claim 16, wherein the line interface comprises a physical interface, a network interworking, and a connectivity engine.

18. The input/output module of Claim 16, wherein the line interface is operable to convert information received from an access technology into a core cell transfer format.

19. The input/output module of Claim 18, wherein the access technology comprises frame relay.

20. The input/output module of Claim 18, wherein the access technology comprises asynchronous transfer mode.

21. The input/output module of Claim 18, wherein the core cell transfer format comprises asynchronous transfer mode.

22. The input/output module of Claim 16, wherein the data interconnect comprises:

two lines operable to couple the to-switch port processor of the input/output module to the switch fabric of the switch control module; and

two lines operable to couple the from-switch port processor of the input/output module to the switch fabric of the switch control module.

23. The input/output module of Claim 16, wherein the data interconnect comprises:

two differential emitter coupled logic lines operable to couple the to-switch port processor of the input/output module to the switch fabric of the switch control module; and

two differential emitter coupled logic lines operable to couple the from-switch port processor of the input/output module to the switch fabric of the switch control module.

24. The input/output module of Claim 16, wherein the switch control module further comprises a plurality of multipoint topology controllers coupled to the bandwidth arbiter, each multipoint topology controller operable to couple to at least one input/output module, the control interconnect comprising:

four lines operable to couple the to-switch port processor of the input/output module to an associated multipoint topology controller of the switch control module;

two lines operable to couple the from-switch port processor of the input/output module to an associated multipoint topology controller of the switch control module; and

one line operable to couple the to-switch port processor of the input/output module to the bandwidth arbiter of the switch control module.

25. The input/output module of Claim 16, further comprising:

a redundant data interconnect coupled to the to-switch port processor and the from-switch port processor, the redundant data interconnect operable to couple to a switch fabric of a redundant switch control module; and

a redundant control interconnect coupled to the to-switch port processor and the from-switch port processor, the redundant control interconnect operable to couple to a bandwidth arbiter of a redundant switch control module.

26. The input/output module of Claim 25, wherein the redundant data interconnect comprises:

two lines operable to couple the to-switch port processor of the input/output module to the switch fabric of the redundant switch control module; and

two lines operable to couple the from-switch port processor of the input/output module to the switch fabric of the redundant switch control module.

27. The input/output module of Claim 25, wherein the redundant data interconnect comprises:

two differential emitter coupled logic lines operable to couple the to-switch port processor of the input/output module to the switch fabric of the redundant switch control module; and

two differential emitter coupled logic lines operable to couple the from-switch port processor of the input/output module to the switch fabric of the redundant switch control module.

28. The input/output module of Claim 25, wherein the redundant switch control module further comprises a plurality of multipoint topology controllers coupled to the bandwidth arbiter of the redundant switch control module, each multipoint topology controller operable to couple to at least one input/output module, the redundant control interconnect comprising:

four lines operable to couple the to-switch port processor of the input/output module to an associated multipoint topology controller of the redundant switch control module;

two lines operable to couple the from-switch port processor of the input/output module to the associated multipoint topology controller of the redundant switch control module; and

one line operable to couple the to-switch port processor of the input/output module to the bandwidth arbiter of the redundant switch control module.

29. An input/output module operable to couple to a switch control module having a switch fabric, the input/output module comprising:

a cell flow processor;

a data interconnect coupled to the cell flow processor, the data interconnect operable to couple to the switch fabric of the switch control module; and

a control interconnect coupled to the cell flow processor, the control interconnect operable to couple to the switch fabric.

30. The input/output module of Claim 29, further comprising:

a redundant data interconnect coupled to the cell flow processor, the redundant data interconnect operable to couple to a switch fabric of a redundant switch control module; and

a redundant control interconnect coupled to the cell flow processor, the redundant data interconnect operable to couple to a switch fabric of a redundant switch control module.

31. The input/output module of Claim 29, further comprising a line interface.

32. The input/output module of Claim 31, wherein the line interface is operable to convert information received from an access technology into a core cell transfer format.

33. The input/output module of Claim 31, wherein the access technology comprises frame relay.

34. The input/output module of Claim 31, wherein the access technology comprises asynchronous transfer mode.

35. The input/output module of Claim 31, wherein the core cell transfer format comprises asynchronous transfer mode.

36. The input/output module of Claim 29, further comprising a line interface having a physical interface, a network interworking, and a connectivity engine.

37. A switch control module operable to couple to a plurality of input/output modules, the switch control module comprising:

a bandwidth arbiter;

a data crossbar coupled to the bandwidth arbiter;

a plurality of data interconnects coupled to the data crossbar, each data interconnect operable to couple to a corresponding input/output module; and

a plurality of control interconnects coupled to the bandwidth arbiter, each control interconnect operable to couple to a corresponding input/output module.

38. The switch control module of Claim 37, wherein each input/output module comprises a to-switch port processor and a from-switch port processor, each data interconnect comprising:

two lines coupled to the data crossbar of the switch control module, the two lines operable to couple to the to-switch port processor of the corresponding input/output module; and

two lines coupled to the data crossbar of the switch control module, the two lines operable to couple to the from-switch port processor of the corresponding input/output module.

39. The switch control module of Claim 37, wherein each input/output module comprises a to-switch port processor and a from-switch port processor, each data interconnect comprises:

two differential emitter coupled logic lines coupled to the data crossbar of the switch control module, the two lines operable to couple to the to-switch port processor of the corresponding input/output module; and

two differential emitter coupled logic lines coupled to the data crossbar of the switch control module, the two lines operable to couple to the from-switch port processor of the corresponding input/output module.

40. The switch control module of Claim 37, further comprising a plurality of multipoint topology controllers coupled to the bandwidth arbiter, each control interconnect comprises:

four lines operable to couple the to-switch port processor of the corresponding input/output module to an associated multipoint topology controller of the switch control module;

two lines operable to couple the from-switch port processor of the corresponding input/output module to the associated multipoint topology controller of the switch control module; and

one line operable to couple the to-switch port processor of the corresponding input/output module to the bandwidth arbiter of the switch control module.

41. The switch control module of Claim 37, further comprising:

a to-switch port processor;

a from-switch port processor;

a redundant data interconnect coupled to the to-switch port processor and the from-switch port processor, the redundant data interconnect operable to couple to a data crossbar of a redundant switch control module; and

a redundant control interconnect coupled to the to-switch port processor and the from-switch port processor, the redundant control interconnect operable to couple to a bandwidth arbiter of the redundant switch control module.

42. The switch control module of Claim 41, wherein the redundant data interconnect comprises:

two lines operable to couple the to-switch port processor of the switch control module to the data crossbar of the redundant switch control module; and

two lines operable to couple the from-switch port processor of the switch control module to the data crossbar of the redundant switch control module.

43. The switch control module of Claim 41, wherein the redundant data interconnect comprises:

two differential emitter coupled logic lines operable to couple the to-switch port processor of the switch control module to the data crossbar of the redundant switch control module; and

two differential emitter coupled logic lines operable to couple the from-switch port processor of the switch control module to the data crossbar of the redundant switch control module.

44. The switch control module of Claim 41, wherein the redundant switch control module further comprises a plurality of multipoint topology controllers coupled to the bandwidth arbiter of the redundant control module, the redundant control interconnect comprising:

four lines operable to couple the to-switch port processor of the input/output module to an associated multipoint topology controller of the redundant switch control module;

two lines operable to couple the from-switch port processor of the input/output module to the associated multipoint topology controller of the redundant switch control module; and

one line operable to couple the to-switch port processor of the input/output module to the bandwidth arbiter of the redundant switch control module.

45. An input/output module operable to couple to a switch control module having a switch fabric, the input/output module comprising:

a to-switch port processor;

a from-switch port processor;

a line interface coupled to the to-switch port processor and the from-switch port processor, the line interface operable to convert information received from an access technology into a core cell transfer format for delivery to the to-switch port processor, the line interface further operable to convert information in a core cell transfer format received from the from-switch port processor into a format for the access technology;

a data interconnect coupled to the to-switch processor and the from-switch processor, the data interconnect comprising two differential emitter coupled logic lines operable to couple the to-switch port processor of the input/output module to the switch fabric of the switch control module, the data interconnect further comprising two differential emitter coupled logic lines operable to couple the from-switch port processor of the input/output module to the switch fabric of the switch control module; and

a control interconnect coupled to the to-switch port processor and the from-switch port processor, the control interconnect comprising four lines operable to couple the to-switch port processor of the input/output module to a multipoint topology controller in the switch fabric of the switch control module, the control interconnect further comprising two lines operable to couple the from-switch port processor of the input/output module to the multipoint

topology controller of the switch control module, the control interconnect further comprising one line operable to couple the to-switch port process of the input/output module to a bandwidth arbiter in the switch fabric of the switch control module.

46. The input/output module of Claim 45, wherein the line interface comprises a physical interface, a network interworking, and a connectivity engine.

47. The input/output module of Claim 45, wherein the access technology comprises frame relay.

48. The input/output module of Claim 45, wherein the access technology comprises asynchronous transfer mode.

49. The input/output module of Claim 45, wherein the core cell transfer format comprises asynchronous transfer mode.

50. The input/output module of Claim 45, further comprising:

a serializer coupled to the to-switch port processor, the serializer operable to convert an n-bit word received from the to-switch port processor into serial data for transmission using the data interconnect; and

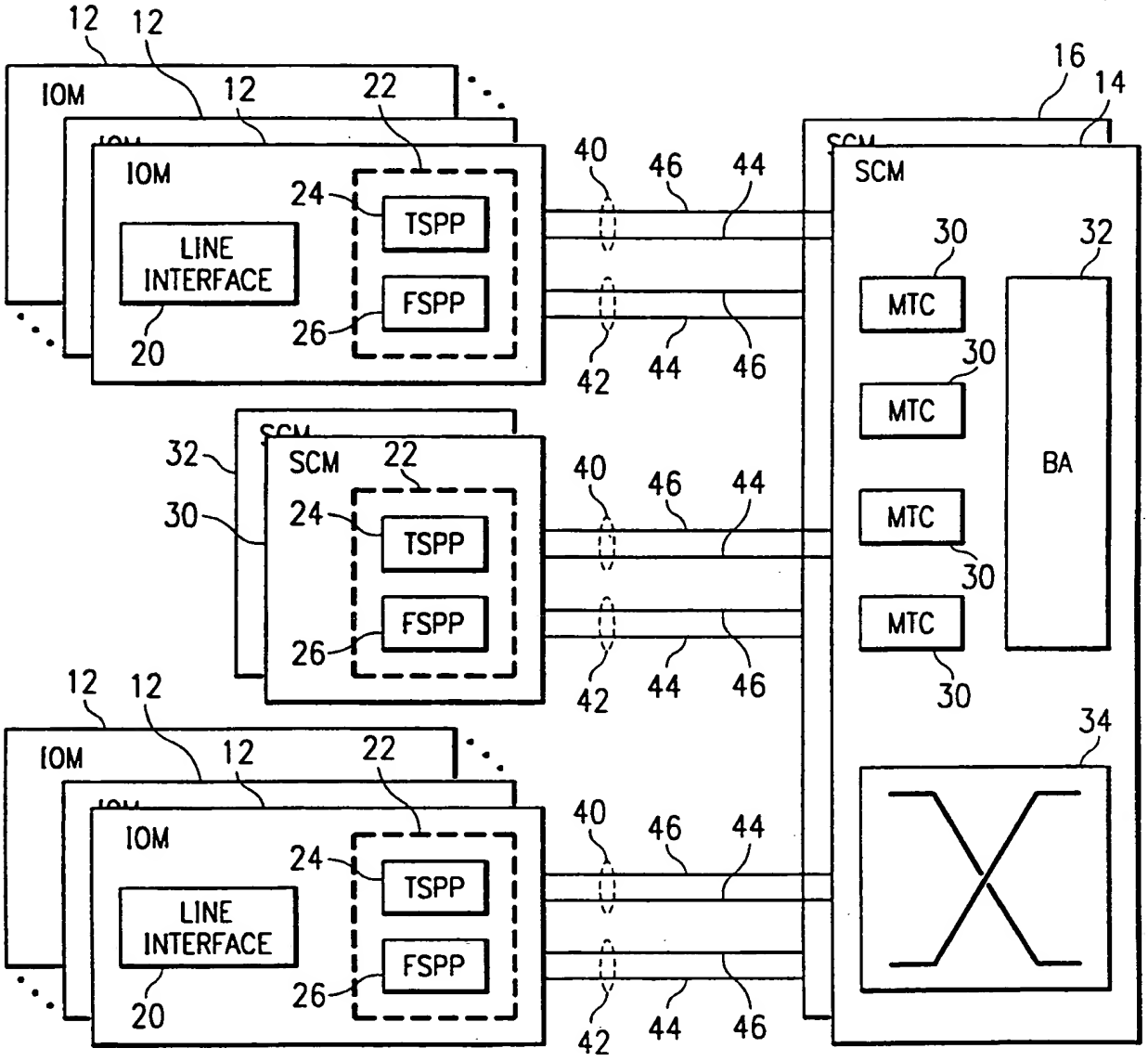
a deserializer coupled to the from-switch port processor, the deserializer operable to convert the serial data received from the data interconnect into an n-bit word for delivery to the from-switch port processor.

51. The input/output module of Claim 50, wherein the serializer and the deserializer support a fiber channel interface.

52. The input/output module of Claim 45, further comprising:

a redundant data interconnect coupled to the to-switch port processor and the from-switch port processor, the redundant data interconnect comprising two differential emitter coupled logic lines operable to couple the to-switch port processor of the input/output module to a switch fabric of a redundant switch control module, the redundant data interconnect further comprising two differential emitter coupled logic lines operable to couple the from-switch port processor of the input/output module to the switch fabric of the redundant switch control module; and

a redundant control interconnect coupled to the to-switch port processor and the from-switch port processor, the redundant control interconnect comprising four lines operable to couple the to-switch port processor of the input/output module to a multipoint topology controller in the switch fabric of the redundant switch control module, the control interconnect further comprising two lines operable to couple the from-switch port processor of the input/output module to the multipoint topology controller of the redundant switch control module, the control interconnect further comprising one line operable to couple the to-switch port processor of the input/output module to a bandwidth arbiter in the switch fabric of the redundant switch control module.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42
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MTC
32
SCM
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BA
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LINE INTERFACE
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42
44
46

FIG. 1

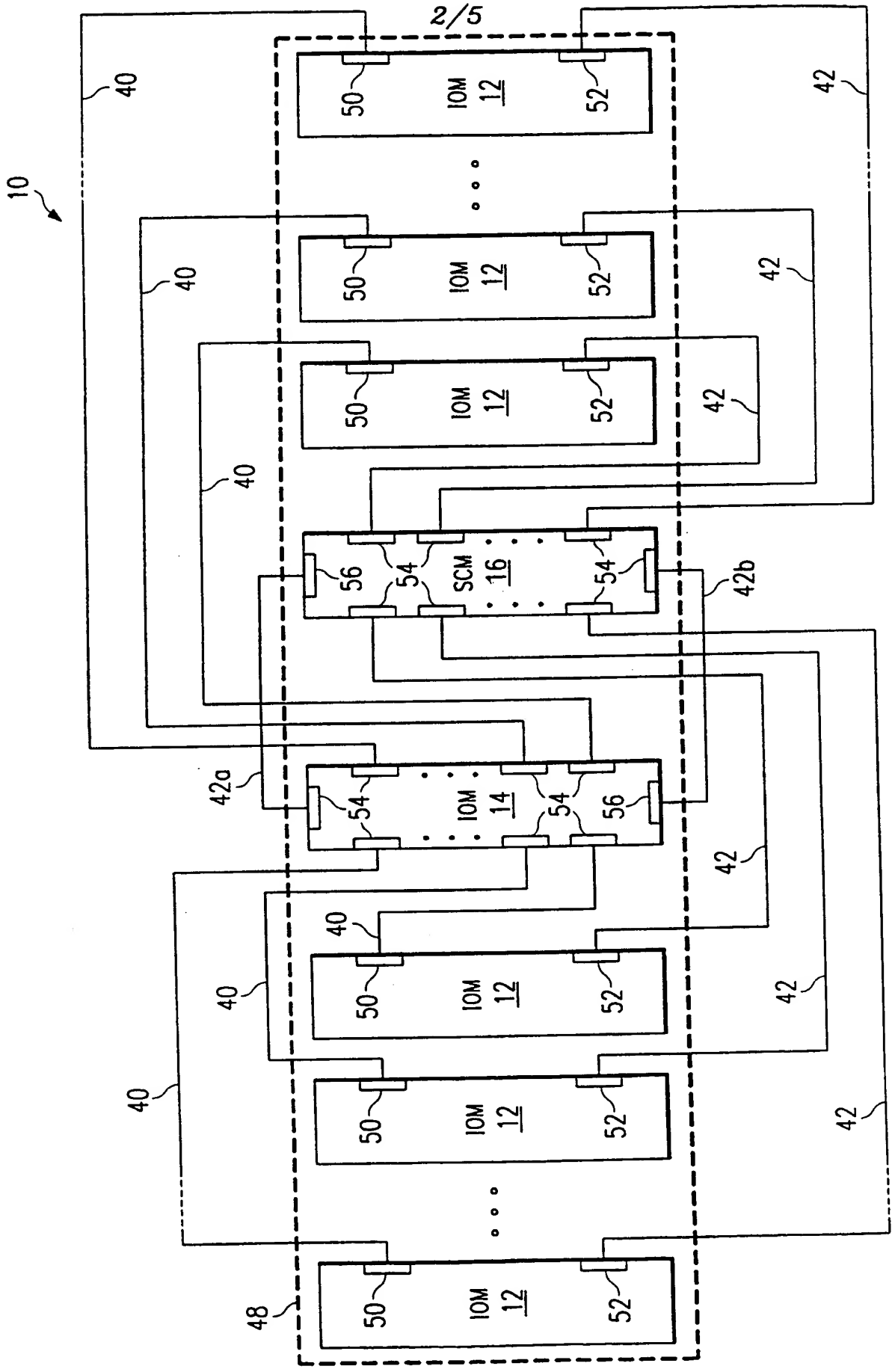
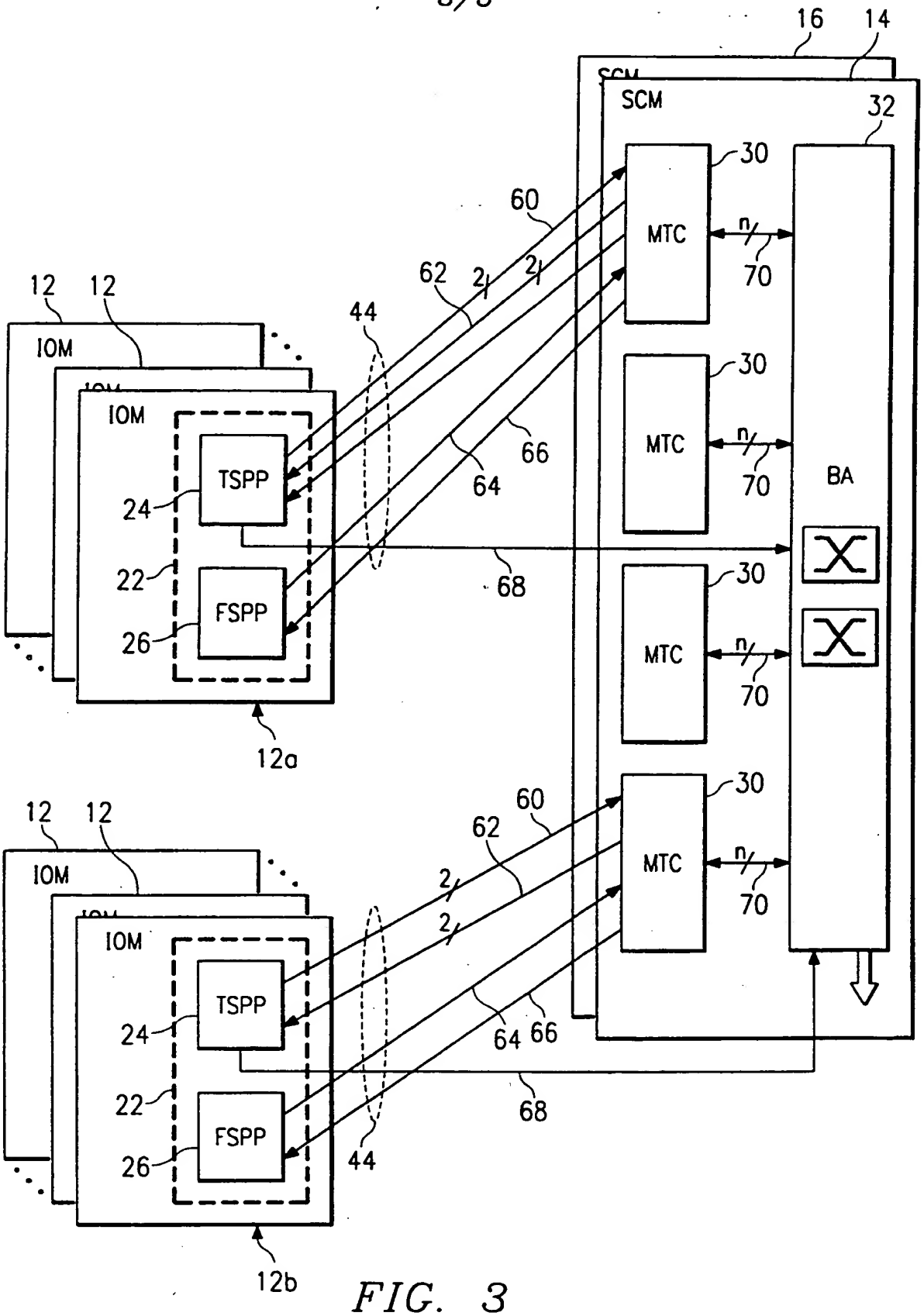


FIG. 2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MTC
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2
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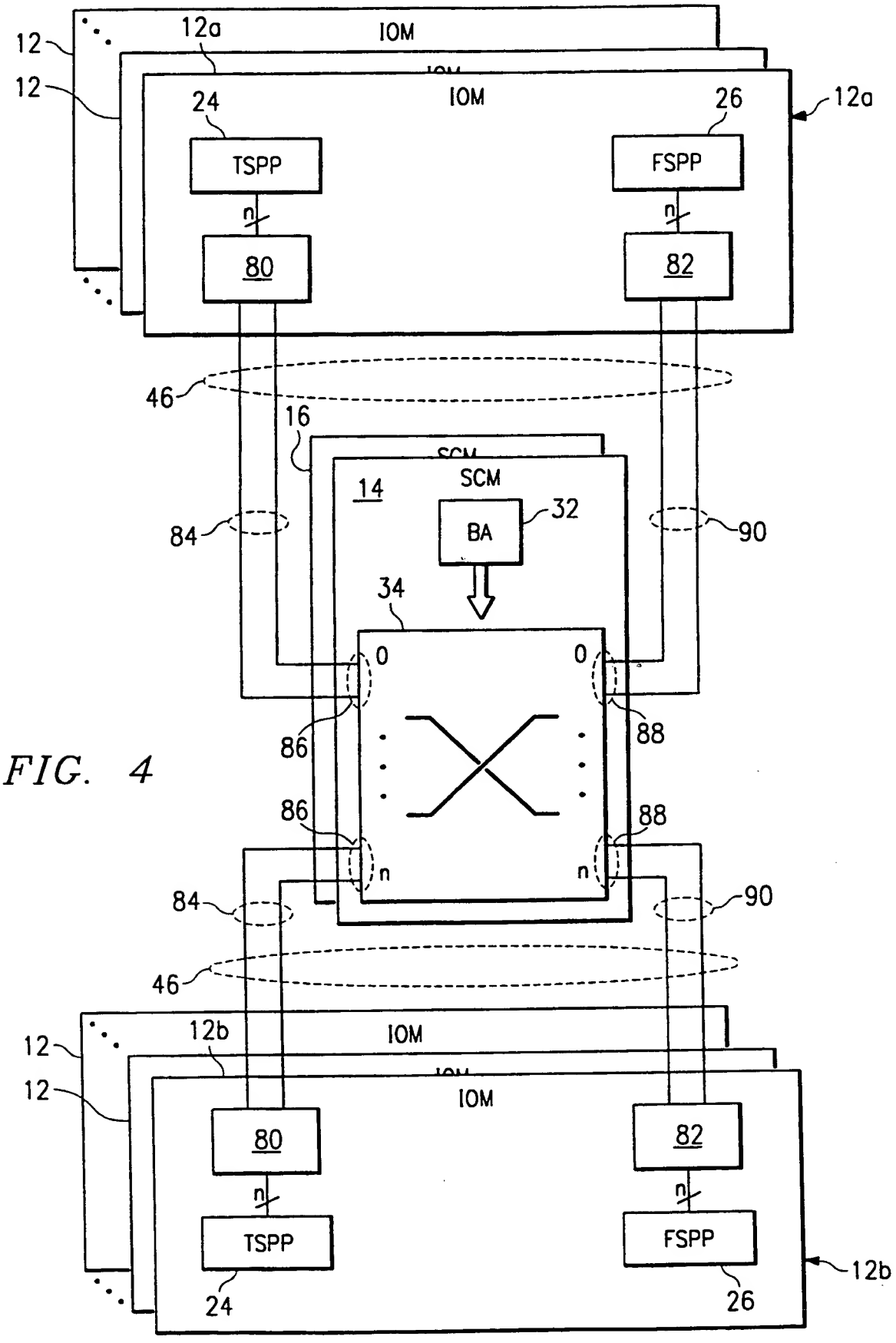
26
64
66
68
BA
12a
12b

FIG. 3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12
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IOM
26
12a
TSPP
FSPP
n
n
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82
46
16
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88
n
n
84
90
46
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IOM
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IOM
80
82
n
n
TSPP
FSPP
12b
24
26

FIG. 4

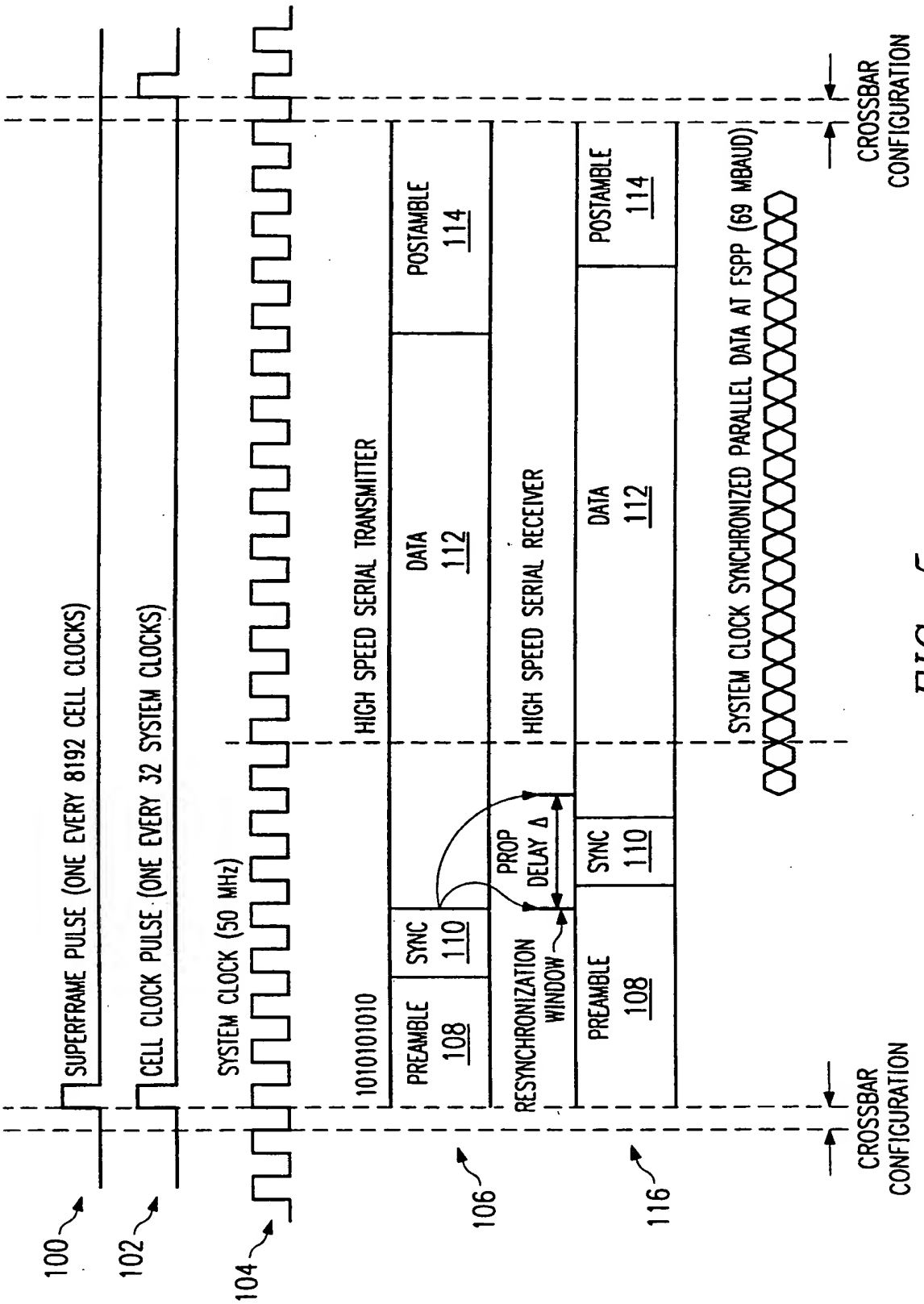
SUPERFRAME PULSE (ONE EVERY 8192 CELL CLOCKS)
CELL CLOCK PULSE (ONE EVERY 32 SYSTEM CLOCKS)
SYSTEM CLOCK (50 MHz)
1010101010
HIGH SPEED SERIAL TRANSMITTER
PREAMBLE 108
SYNC 110
DATA 112
POSTAMBLE 114
RESYNCHRONIZATION WINDOW
PROP DELAY Δ
HIGH SPEED SERIAL RECEIVER
PREAMBLE 108
SYNC 110
DATA 112
POSTAMBLE 114
SYSTEM CLOCK SYNCHRONIZED PARALLEL DATA AT FSPP (69 MBAUD)
CROSSBAR CONFIGURATION
CROSSBAR CONFIGURATION
100
102
104
106
116

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/11946

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G06F 15/00, 15/76, 15/80; H04Q 11/04; G06F 7/00
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/200.02, 200.13, 200.15, 311, 312, 849; 370/60.1, 85.11, 94.3; 340/825.89

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, search terms: crossbar switches, serial control, multipoint topology, plurality or multiple modules or devices or units

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 3,974,343 (CHENEY et al) 10 August 1976, Fig 1A, the abstract and col. 11 lines 9-62	1-52
A	US, A, 4,821,034 (ANDERSON et al) 11 April 1989, Fig. 15, the abstract, col. 5 lines 23-65, and col. 32 lines 39-60	1-52
A	US, A, 5,420,988 (ELLIOTT) 30 May 1995, Fig. 1, the abstract and col. 2 line 58 - col. 3 line 50	1-52
A, P	US, A, 5,506,956 (COHEN) 09 April 1996, Fig. 7, the abstract and col. 19 line 31 - col. 20 line 23	1-52

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 20 August 1996	Date of mailing of the international search report 17 SEP 1996
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer Thomas C. Lee Telephone No. (703) 305-9717

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/11946

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A,P	US, A, 5,524,113 (GADDIS) 04 June 1996, Fig. 4, the abstract, col. 4 line 45 - col. 5 line 9, and col. 12 lines 28-59	1-52

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/11946

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

395/200.02, 200.13, 200.15, 311, 312, 849; 370/60.1, 85.11, 94.3; 340/825.89